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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,193	08/18/2003	Azeez Bhavnagarwala	YOR920030289US1 (8728-635	3651

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EXAMINER	
WEST, JEFFREY R	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,193	BHAVNAGARWALA ET AL.	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *20-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,26 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-19, 26, and 27, drawn to a method, and/or program of instructions for carrying out a method, for characterizing mismatch, classified in class 702, subclass 117.

II. Claims 20-25, drawn to a testing apparatus for characterizing mismatch, classified in class 324, subclass 769.

2. The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the process for characterizing mismatch can be practiced by an other materially different apparatus such as a single measuring device that obtains and processes a DC voltage characteristic without the use of a plurality of circuits with a corresponding multiplexer.

3. Because these inventions are distinct for the reasons given above and

have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Mr. Frank DeRosa on January 13, 2005 a provisional election was made with traverse to prosecute the invention of group I, claims 1-19, 26, and 27. Affirmation of this election must be made by applicant in replying to this Office action. Claims 20-25 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

6. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

7. The drawings are objected to because of the following informalities:

Figures 5(a), 6, and 7(a) contain numerals I, II and III, respectively. Since there is no reference to these numerals in the specification, they should be removed.

Figures 8 and 9 are objected to because they do not contain descriptive titles. It is suggested that Applicant include titles to the graphs reflecting the information they present, specifically, on page 34, lines 12-17 and page 35, lines 4-9.

8. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any

required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

9. The abstract of the disclosure is objected to because its length exceeds the 150-word limit. Correction is required. See MPEP § 608.01(b).

10. The disclosure is objected to because of the following informalities:

On page 14, line 23, "Fig. 15 is a diagram" should be ---Fig. 15(a) and (b) are diagrams---.

On page 15, line 8, "measure and characterized" should be ---measure and characterize---.

On page 18, line 18, "AS" should be ---As---.

Appropriate correction is required.

Claim Objections

11. Claims 1, 4-6, 10-14, 19, 26, and 27 are objected to because of the following informalities:

In claim 1, line 7, to avoid problems of antecedent basis, "the device pair" should be ---the pair of semiconductor devices---.

In claim 4, line 2, to avoid problems of antecedent basis, "the device pair" should be ---the pair of semiconductor devices---.

In claim 4, line 3, to avoid problems of antecedent basis, "said data" should be ---said DC voltage characteristic data---.

In claim 5, line 2, to avoid problems of antecedent basis, "the device pair" should be ---the pair of semiconductor devices---.

In claim 6, line 2, to avoid problems of antecedent basis, "the device pair" should be ---the pair of semiconductor devices---.

In claim 10, line 7, to avoid problems of antecedent basis in line 11, "a distribution" should be ---one or more distributions---.

In claim 10, line 9, to avoid problems of antecedent basis, "the device pair" should be ---the selected device pair---.

In claim 10, line 10, to avoid problems of antecedent basis in line 14, "a Vt variation" should be ---one or more Vt variations---.

In claim 11, lines 2-3, to avoid problems of antecedent basis, "a selected device pair" should be ---one or more selected device pairs---.

In claim 12, lines 2-3, to avoid problems of antecedent basis, "a selected device pair" should be ---one or more selected device pairs---.

In claim 13, lines 2-3, to avoid problems of antecedent basis, "a selected device pair" should be ---one or more selected device pairs---.

In claim 14, line 4, to avoid problems of antecedent basis, "subthreshold region" should be ---subthreshold voltage region---.

In claim 19, line 2, to avoid problems of antecedent basis, "a Vt variations" should be ---one or more Vt variations---.

In claim 26, line 10, to avoid problems of antecedent basis, "the device pair" should be ---the pair of semiconductor devices---.

In claim 27, line 8, to avoid problems of antecedent basis, "the device pair" should be ---the selected device pair---.

In claim 27, line 10, to avoid problems of antecedent basis in line 14, "a distribution" should be ---one or more distributions---.

In claim 27, line 13, to avoid problems of antecedent basis in line 17, "a Vt variation" should be ---one or more Vt variations---.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claims 7-9, and 13-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 is considered to be vague and indefinite because it recites the confusing language, "further comprising the step of determining a variation in a device characteristic for a device of an integrated circuit comprising the device pair the distribution of variation of device mismatch for the device pair." In this limitation it is unclear as to what "the distribution of variation of device mismatch for the device pair" is further limiting.

Claim 8 is rejected under 35 U.S.C. 112, second paragraph, because it recites "The method of claim 8" and therefore depends from itself. For the remainder of this Office Action it is assumed that claim 8 depends from claim 7 rather than claim 8.

Claim 8 is further considered to be vague and indefinite because it recites, "for each device of the integrated circuit". Parent claims 1 and 7, however, do not define a plurality of devices of the integrated circuit, but instead only define a "pair of semiconductor devices". Therefore, it is unclear to one having ordinary skill in the art whether "each device of the integrated circuit" refers to the "pair of semiconductor devices" or additional devices not defined.

Claim 9 is rejected under 35 U.S.C. 112, second paragraph, because it recites, "wherein the devices comprise transistors". Parent claims 1, 7 and 8, however, already define "device mismatch", "the device pair", and "each device of the integrated circuit". It is therefore unclear to one having ordinary skill in the art as to which devices "the devices" refer.

Claim 13 is considered to be vague and indefinite because it recites "repeating steps (i) – (iii) for each of a plurality of separate device pairs of the first and second transistors". It is unclear to one having ordinary skill in the art, however, how the first and second transistors can be used to form a plurality of separate device pairs.

Claims 14-17 are rejected under 35 U.S.C. 112, second paragraph, because they incorporate the lack of clarity present in parent claim 13.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 1-3, 6-10, 12, 19, 26, and 27, as may best be understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Bastos et al., "Mismatch characterization of small size MOS transistors".

Bastos discloses a method for characterizing device mismatch in a semiconductor integrated circuit (page 271, column 1, "Introduction", lines 1-2), comprising the steps of obtaining DC voltage characteristic data (i.e. DC drain current based on DC gate voltage) for a pair of semiconductor devices by varying a transistor input gate voltage (page 271, column 2, "Measurement Methodology", lines 6-18 and page 272, column 1, "The Extraction Algorithms", lines 13-15), processing the DC voltage characteristic data to determine a distribution of device mismatch between devices comprising the device pair (page 272, columns 1-2, "The Extraction Algorithms", lines 1-15 and 32-36), determining a threshold voltage variation of the transistors in the integrated circuit using one or more determined distributions of mismatch for selected device pairs (page 272, column 2, "Algorithm Validation", lines 1-16), and characterizing random variations of the integrated circuit (i.e. random

variations in transistor dimensions) using one or more determined threshold voltage variations of transistors of the integrated circuit (page 274-275, "Mismatch Dependence on Transistor Size").

Bastos discloses that the device pair comprises two neighboring, similar, transistors (page 272, column 1, "The Extraction Algorithms", lines 13-15) and that the distribution of device mismatch comprises a distribution of threshold voltage mismatch (page 272, columns 1-2, "The Extraction Algorithms", lines 1-15 and 32-36).

Bastos discloses that the step of obtaining DC voltage characteristic data for the device pair comprises separately measuring DC voltage characteristic data for each of a plurality of similar device pairs (page 271, column 2, "Measurement Methodology", lines 5-6) and determining a variation in a device characteristic for a device of an integrated circuit comprising the device pair (page 274-275, "Mismatch Dependence on Transistor Size") as well as assessing random variation of device mismatch of the semiconductor integrated circuit using variations in the device characteristic for each of a plurality of devices of the integrated circuit as determined from repeatedly determining distributions of variation of device mismatch for device pairs within the integrated circuit (page 271, "The Test Chip" and page 272, column 2, "Algorithm Validation", lines 11-19).

Bastos also discloses that the distribution of threshold mismatch between the first and second transistors is between first and second NFETs (page 272, column 2, "Algorithm Validation", lines 11-14).

Bastos discloses that the step of determining a voltage threshold variation of transistors in the integrated circuit comprises determining a standard deviation of voltage threhsold variation of the transistors (page 272, column 2, "Algorithm Validation", lines 1-16)

Bastos further discloses a plurality of programmed algorithms for execution by a test system and therefore it is considered inherent that some type of program storage device readable by the test system tangibly embodying the algorithms is present (page 271, column 2, "Measurement Methodology", lines 1-2 and page 272, column 1, "The Extraction Algorithms", lines 1-3).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bastos in view of U.S. Patent No. 6,731,916 to Haruyama.

As noted above, the invention of Bastos teaches many of the features of the claimed invention and while Bastos does obtain DC voltage characteristic data for a pair of transistors, Bastos does not specify retrieving this data from a database.

Haruyama teaches a power amplifying apparatus for a mobile phone including an FET with a bias current setting circuit (column 3, lines 9-11) and a memory/database (column 3, lines 11-13) wherein voltage characteristic data for the FET is stored in the memory/database (column 3, lines 14-20) and, when needed, is retrieved from the memory/database (column 3, lines 42-47).

It would have been obvious to one having ordinary skill in the art to modify the invention of Bastos to include retrieving the DC voltage characteristic data from a database, as taught by Haruyama, because Haruyama suggests that the combination would have saved time an effort by storing the characteristic data in a database (column 3, lines 14-20 and column 3, lines 42-47) thereby not requiring the process of measuring the characteristic data each time the mismatch is to be determined in the invention of Bastos.

18. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bastos in view of Conti et al., "Test structure for mismatch characterization of MOS transistors in subthreshold regime".

As noted above, the invention of Bastos teaches many of the features of the claimed invention and while Bastos does teach obtaining DC voltage characteristic of a transistor pair, Bastos teaches obtaining the DC voltage characteristic for a transistor pair biased in the saturation region rather than the subthreshold region.

Conti teaches a test structure for threshold voltage mismatch comprising obtaining subthreshold DC voltage characteristic data for adjacent transistor devices (page 173, column 1, "Introduction, lines 1-9 and page 173, column 2, "Mismatch Model", lines 9-13) by biasing the transistors in a subthreshold region through application and maintenance of corresponding gate voltages (page 173, "Test Circuits" and page 174, column 1, lines 1-7).

It would have been obvious to one having ordinary skill in the art to modify the invention of Bastos to include obtaining the DC voltage characteristic for a transistor pair biased in the subthreshold region, as taught by Conti, because, as suggested by Conti, the combination would have improved the analysis of mismatch by providing a better estimates of threshold mismatch (page 174, column 1, lines 1-7).

19. Claims 13-16, as may best be understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bastos in view of Conti and further in view of U.S. Patent No. 4,851,768 to Yoshizawa et al.

As noted above, the invention of Bastos and Conti teaches many of the features of the claimed invention, and while the invention of Bastos and Conti does teach biasing a transistor pair in a subthreshold region using proper varying gate voltages and obtaining a DC voltage characteristic of the transistor pair in order to determine threshold voltage mismatch for each of the transistor pairs, the combination does not specify that the DC voltage characteristic is obtained by measuring an output voltage of a node between

the first and second transistors and determining a distribution of input voltage for the given output voltage to determine the threshold voltage mismatch.

Yoshizawa teaches a characteristic test apparatus for an electronic device comprising a transistor pair configured with a node for measuring an output voltage, that varies as a function of the input voltage, between the first and second transistors (Figure 2a) wherein a varying/distribution of input voltages are applied to obtain voltage output to determine a threshold voltage as part of the DC voltage characteristic (column 4, lines 59-67 and column 6, lines 6-14).

It would have been obvious to one having ordinary skill in the art to modify the invention of Bastos and Conti to specify that the DC voltage characteristic is obtained by determining a distribution of input voltage for a given output voltage, as taught by Yoshizawa, because the invention of Bastos and Conti obtains a transistor characteristic to determine a threshold voltage and Yoshizawa suggests a similar method for determining such a transistor characteristic that would have simplified the characteristic determination by measuring two voltages, rather than requiring complex measurements of a current voltage relationship, that, as suggested by Yoshizawa, would have complied with conventional means of measuring transistor characteristics using the input and output voltages (column 4, lines 59-68).

20. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bastos in view of U.S. Patent No. 6,181,621 to Lovett.

As noted above, the invention of Bastos teaches many of the features of the claimed invention and while Bastos does teach characterizing mismatch in a semiconductor integrated circuit, Bastos does not specify that the integrated circuit be an SRAM.

Lovett teaches a threshold voltage mismatch compensated sense amplifier for SRAM memory arrays comprising means for obtaining threshold voltage mismatch information in a SRAM (column 1, lines 6-10 and column 2, lines 7-15).

It would have been obvious to one having ordinary skill in the art to modify the invention of Bastos to specify that the integrated circuit be an SRAM, as taught by Lovett, because Lovett suggests that SRAM devices are devices that are greatly affected by threshold mismatches due the size constraints of such SRAMs (column 3, line 65 to column 4, line 7) and therefore the combination would have provided greater utility in the invention of Bastos by applying the method to the SRAM devices.

Further, it has been held that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). In the instant case the structure of Bastos is capable of characterizing transistor

mismatch in any of a wide variety of integrated circuits, such as an SRAM, and therefore meets the claim.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lakshmikumar et al., "Characterization and Modeling of Mismatch in MOS Transistors for Precision Analog Design" teaches the determination of physical causes of mismatch for both p and n-channel devices.

Pavasovic et al., "Characterization of Subthreshold MOS Mismatch in Transistors for VLSI Systems" teaches the determination of subthreshold mismatch in transistor pairs.

Bhavnagarwala et al., "The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability" teaches the determination of threshold voltage distribution functions for SRAM devices.

U.S. Patent No. 6,628,146 to Tam teaches a comparator circuit and method that determines a distribution of Vin for Vout of a transistor pair.

U.S. Patent No. 6,161,213 to Lofstrom teaches a system for providing an integrated circuit with a unique identification by plotting a distribution of threshold voltage mismatch between pairs of MOSFETs.

22. Any inquiry concerning this communication or earlier communications from

the examiner should be directed to Jeffrey R. West whose telephone number is (571)272-2226. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571)272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jrw
January 23, 2005

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